IEEE POWER ELECTRONICS REGULAR PAPER

Multilevel Converters with Symmetrical Half-Bridge Submodules and Sensorless Voltage Balance

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***Abstract*—H-bridge-based multilevel converters (e.g., cascaded H-bridge converters) benefit from modularity and scalability. However, they suffer from the complexity and costs associated with a large count of semiconductor switches, together with their drivers and peripheral circuits, as well as higher conduction losses as compared to half-bridge-based counterparts, as two switches in each submodule must simultaneously conduct to provide a current path. To reduce the number of active switch semiconductors and conduction losses, this paper proposes novel multilevel converters with symmetrical half-bridge submodules. The symmetrical half-bridge submodule features a bipolar voltage output, a reduced switch count, and simplicity. Further, this paper proposes a sensorless voltage balance scheme that successfully gets rid of capacitor voltage mismatch problems through diodes and submodule parallelization. This scheme can greatly reduce capacitor voltage ripples, thereby allowing the saving of dc capacitances, particularly in the case of numerous submodules. Finally, simulation and experimental results validate the superiority of the proposed multilevel converters and voltage balance scheme.**

Index terms—Cascaded H-bridge (CHB), half-bridge, modular multilevel converter (MMC), multilevel converter, sensorless voltage balance.

I. Introduction

The development of multilevel converters promises to advance high-voltage dc (HVdc) and ac (HVac) transmissions [1], medium voltage motor drive (e.g., automotive propulsion and marine drive) [2], renewable generation [3], power quality enhancement [4], medical applications such as pulse synthesizers for noninvasive magnetic brain stimulation [5], energy storage integration, and electric vehicles [6]. Attractive features of multilevel converters include the use of low-voltage semiconductors for high-voltage treatments, high power quality, the possibility of removing passive filters [7], low electromagnetic interference noises (due to reduced voltage and current changing rates), high reliability and redundancy, and diminished common mode problems [6]. Despite these identified advantages, multilevel converters are burdened by the complexity and costs associated with large amounts of active and passive components. Such shortcomings push forward the research of simpler multilevel converters [8].

Manuscript received December 13, 2019; revised April 06, 2020; accepted June 02, 2020. This work was supported by the National Science Foundation under grant No. 1608929.

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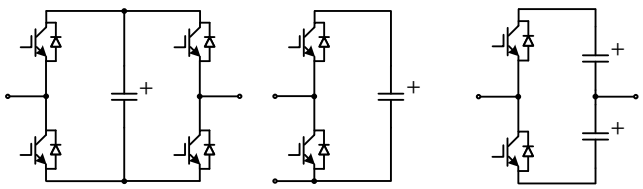
To date, cascaded bridge, diode-clamped, and flying capacitor converters are proving to be appealing choices [9−11]. Cascaded bridge converters stand out among them due mostly to the removal of additional diodes or balancing capacitors, modularity, and scalability. Assembling cascaded bridge converters into larger structures, one can readily derive the well-known modular multilevel converter (MMC) [12]. Recent years witness continuing progress in the commercialization and development of MMCs [13].

Since its inception, the research on the submodules of cascaded bridge converters and MMCs continues its upward trend [13−15]. This is understandable, as submodules greatly impact the cost and performance of multilevel power conversion systems. For selection of submodules, the H-bridge circuit shown in Fig. 1(a) is well-proven. It enjoys the benefits of a bipolar voltage output, a standard structure, and short-circuit protection in MMCs [13]. However, H-bridge-based multilevel converters suffer from the complexity and costs associated with a large count of semiconductor switches paired with their drivers and peripheral circuits, which are the common drawbacks of multilevel converters. Another key concern appears to be higher conduction losses as compared to half-bridge-based counterparts, as two switches in each submodule must conduct to form a current path.

Aiming to address the above-mentioned concerns, the asymmetrical half-bridge submodule depicted in Fig. 1(a) quickly finds its widespread applications in half-bridge and three-phase MMCs [12], [16]. It saves half of switches and dramatically simplifies converter circuits. Nevertheless, this half-bridge submodule allows only a unipolar voltage output, i.e., the dc voltage or zero, thereby failing to operate in cascaded bridge converters and single-phase H-bridge MMCs, where bipolar voltage outputs cannot simply be achieved via the voltage differences between lower and upper arms [14], [17]. As such, H-bridge submodules continue to dominate the application of cascaded bridge converters so that the cascaded H-bridge (CHB) becomes a standard terminology [3], [18].

Novel submodules, such as flying capacitor [14], neutral-point-clamped (NPC) [15], clamp-double [19], double-zero



(a) H-bridge and asymmetrical half-bridge (b) Symmetrical half-bridge

Fig. 1. Schematics of multilevel converter submodules.

[13], mixed half-bridge and H-bridge [15], and double H-bridge submodules [20], were proposed for various purposes, e.g., the increment of voltage levels, short-circuit protection, and parallel connectivity. Although some of these submodules proved to be attractive, they are more complicated than the H-bridge submodule.

In fact, the symmetrical half-bridge submodule illustrated in Fig. 1(b) is a promising alternative to the H-bridge submodule. The benefits of symmetrical half-bridge submodules comprise a marriage of bipolar voltage outputs (featured by H-bridge submodules) and reduced switch counts and conduction losses (possessed by half-bridge submodules). Notably, symmetrical half-bridge converters remain an active area of ongoing research. Their candidate applications include active rectifiers [21], active power filters (APFs) [22], power decoupling circuits [23], unified power quality conditioners (UPQCs) [24], linear compressors [25], etc. Although the symmetrical half-bridge circuit presents a clear advantage from the implementation point of view, it is historically been of little interest in multilevel converters. One major barrier narrowing the application of symmetrical half-bridge submodules to single converters refers to the imbalance of upper and lower capacitor voltages, as will be detailed in Section IV. After removing this barrier, one can reap the advantages of symmetrical half-bridge submodules in multilevel converters.

This paper proposes novel multilevel converters with symmetrical half-bridge submodules and sensorless voltage balance. The rest of this paper is organized as follows. Section II introduces the fundamental operating principles of existing CHB converters and MMCs. Section III introduces the proposed multilevel converters with symmetrical half-bridge submodules. Also, the benefits of half-bridge submodules are highlighted through detailed cost and power loss analyses. Section IV focuses on one major challenge faced by the proposed multilevel converters, i.e. the balance of submodule capacitor voltages. As a solution, it proposes a voltage balance scheme that exploits diodes to achieve submodule parallelization and voltage ripple reduction. Section V presents the simulation and experimental results for verification purposes. Finally, Section VI provides concluding remarks.

II. Fundamental Operating Principles of CHB Converters and MMCs

This section reviews the basic operating philosophy of existing CHB converters and MMCs. It aims to lay the groundwork for the comparison analyses covered in the next section.

For demonstration, Fig. 2 illustrates the schematic diagram of CHB converters or H-bridge-based MMC arms. As noticed, the CHB converter consists of n (n represents a positive integer) H-bridge submodules with their output terminals connected in series. Normally, H-bridge submodules convert their dc terminal voltages v_{dcx} (x = 1, 2, … , or n) into ac terminal voltages through the operation of semiconductor switches. However, it is also possible that multilevel converters output dc voltages [14]. Without loss of generality, we denote the output voltages of individual submodules as v_{acx}.

By means of series connection, the individual submodule voltages v_{acx} are added together, forming an overall output voltage v_{ac}. This overall voltage v_{ac} can be much greater than the individual dc-link voltages v_{dcx}, and thereby allowing the low-voltage semiconductor switches, which are subject to dc voltage stresses, to be suitable for high-voltage applications. In terms of versatility, CHB converters are easily scaled according to the requirement of v_{ac} via the change of submodule numbers. Moreover, as all submodules are identical, CHB converters benefit from modularity. As compared to diode-clamped or flying capacitor converters, CHB converters feature no additional diode or balancing capacitor [2]. In addition, note that either capacitors or batteries can be used in the dc side, their major control difference lies in the regulation of capacitor voltages. In this sense, the capacitors fed by front-end rectifiers are similar to batteries [26]. In the output side (or ac side), either a power grid or an electric load may appear dependent on operating conditions [4], [26].

CHB converters are essentially the arms of H-bridge-based MMCs [17]. To generalize the concept, MMCs are multilevel converters that replace the individual active switches of typical two-level converters, such as symmetrical half-bridge, H-bridge, and three-phase-bridge converters, with cascaded-bridge converters. Referring to Fig. 1(b), one can infer that the half-bridge MMC is derived by replacing the two active switches of the symmetrical half-bridge circuit with two cascaded-bridge converters [12].

There are two important properties of MMCs. One refers to the micro topology or the submodule circuit. The other is related to the macro topology or the basic two-level circuit in support of MMCs [6]. To differentiate these two properties, we use the prefix “half-bridge” to represent basic two-level circuits and the prefix “half-bridge-based” for submodule topologies. Although MMCs allow very flexible operations, they are determined by basic circuits and cascaded-bridge converters, which in turn depend on submodules. As such, the research interest on submodules maintains high [15]. One notable example is the asymmetrical half-bridge submodule shown in Fig. 1(a). Due to their size, cost, and efficiency benefits, asymmetrical half-bridge submodules have been the top option in commercial MMCs for HVDC applications until very recently H-bridge-based MMCs appear. However, the asymmetrical half-bridge submodule features unipolar voltage output and cannot continue to transfer power during dc side short

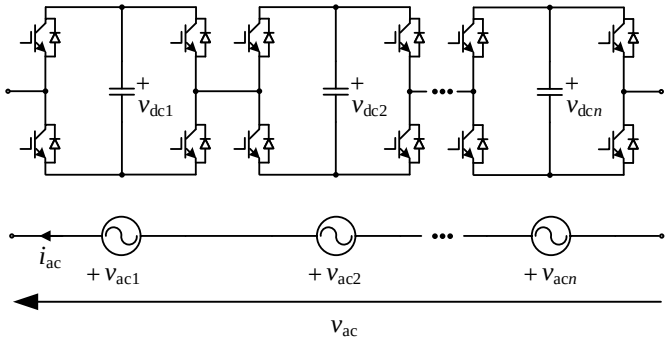


Fig. 2. Schematic of CHB converters or H-bridge-based MMC arms.

circuits. Therefore, they are limited in their applications [17].

III. Proposed Multilevel Converters with Symmetrical Half-bridge Submodules

This section focuses on the principles of the proposed multilevel converters with symmetrical half-bridge submodules. Meanwhile, the benefits of half-bridge submodules are highlighted through comparisons with H-bridge submodules.

A. Operating Principles of the Proposed Multilevel Converters

Recapping that the asymmetrical half-bridge submodule in Fig. 1(a) simplifies MMC circuits at the expense of unipolar outputs, one can further imagine the use of symmetrical half-bridge submodules in Fig. 1(b), whose basic principle is explained as follows. With the upper switch turned on and the lower switch off, the symmetrical half-bridge submodule yields a positive voltage, i.e., the upper capacitor voltage. Alternatively, a negative output or lower capacitor voltage is expected. Combining these two operating modes, the symmetrical half-bridge submodule allows a bipolar voltage output with a simple structure. The proposed cascaded bridge converter or MMC arm with symmetrical half-bridge submodules is shown schematically in Fig. 3. Once again, the overall output v_{ac} is contributed by individual submodule outputs v_{acx} (x = 1, 2, … , or n). In this regard, the proposed cascaded bridge and CHB converters share the same basic operating principles. Next, the benefits of the proposed converters will be disclosed.

B. Cost Analysis

Before conducting a detailed cost analysis, we first analyze the requirement of passive and active components in cascaded bridge converters. Returning to Fig. 2, one can note that a CHB converter with n submodules necessitates 4n active switches, e.g., insulated-gate bipolar transistors (IGBTs) or metal-oxide semiconductor field-effect transistors (MOSFETs), in combination with n dc capacitors. Proceeding to Fig. 3, the proposed cascaded bridge converter with n submodules obviously requires 2n active switches and 2n dc capacitors. In comparison, the proposed converter saves half of switches at the expense of more dc capacitors. Nevertheless, when applied to renewable energy generation, the additional dc capacitors of the proposed converter allow the integration and independent control of more renewable energy resources. If batteries are used in replacement of dc capacitors, the proposed converter allows a finer balance of battery cells. In summary, Table I lists the component comparison results, where the on-state switch refers to the switch that conducts currents, which will be discussed later. It is important to remember that the above comparison holds valid for single-phase converters. In the case of three-phase converters, the numbers of switches, drivers, and dc sources triple, but so do the savings.

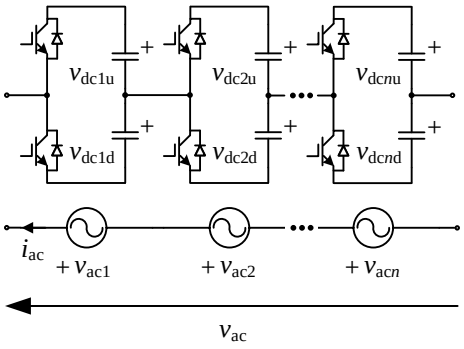


Fig. 3. Schematic of the proposed cascaded bridge converters or MMC arms with symmetrical half-bridge submodules.

Despite the saving with respect to the number of semiconductors, the half-bridge submodule stresses its active switches with double the dc voltages (i.e., $v_{dcxu} + v_{dcxd} = 2v_{dcx} = 2V_{dc}$) as compared to H-bridge submodules. For a fair comparison, switch pairs with twice voltage rating differences and similar other features (e.g., technologies, switching frequency ranges, and current ratings) are documented in Tables II−IV [27−29], where the comparisons cover major active switches, including IGBTs, Si MOSFETs, and gallium nitride (GaN) FETs. It should be mentioned that silicon carbide (SiC) MOSFETs are excluded, because they are currently marketed for one narrow voltage band [30]. By examination of Tables II−IV, the prices of high-voltage switches are always lower than twice the prices of their low-voltage counterparts. In several cases, the price differences between switch pairs are relatively minor or even

Table I. Component comparison between CHB and proposed converters.

Items	CHB converter	Proposed converter
Submodule no.	n	n
Active switch no.	4n	2n
Half-bridge driver no.	2n	n
On-state switch no.	2n	n
Dc source no.	n	2n

Table II. Comparison between Infineon IGBTs.

Products	V_{CEmax}	$V_{CE(sat)}$	I_{Cmax}@100˚	Prices
IKW20N60H3	600 V	1.95 V	20 A	$3.54
IKW25N120H3	1200 V	2.05 V	25 A	$3.54
IKW40N60H3	600 V	1.95 V	40 A	$5.24
IKW40N120H3	1200 V	2.05 V	40 A	$8.48
IKW50N60T	600 V	1.5 V	50 A	$6.29
IKQ50N120CT2	1200 V	1.75 V	50 A	$11.67

Table III. Comparison between Infineon MOSFETs.

Products	V_{DSmax}	$R_{DS(on)}$	I_{Cmax}@25˚	Prices
IRF3703	30 V	2.8 mΩ	210 A	$2.84
IRFS3206	60 V	3 mΩ	210 A	$2.81
IPI80N04S4-03	40 V	3.7 mΩ	80 A	$1.5
IPP80N08S4-06	80 V	5.5 mΩ	80 A	$2.32
IPD50N06S4L-12	60 V	12 mΩ	50 A	$0.91
IPD50N12S3L-15	120 V	15 mΩ	50 A	$1.53

Table IV. Comparison between EPC eGaN FETs.

Products	V_{DSmax}	$R_{DS(on)}$	I_{Cmax}@25°	Prices
EPC2023	30 V	1.45 mΩ	90 A	$7.11
EPC2020	60 V	2.2 mΩ	90 A	$7.28
EPC2024	40 V	1.5 mΩ	90 A	$7.18
EPC2021	80 V	2.5 mΩ	90 A	$7.40

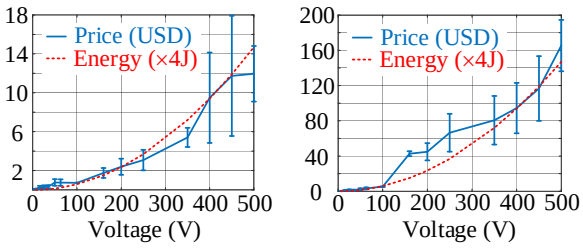
Table V. Infineon IGBT gate drivers.

Products	Types	V_{OFFSET}	Prices
IR2113S	High side and low side	600 V	$4.23
IR2184S	Half-bridge	600 V	$3.32
IR2213SPBF	High side and low side	1200 V	$6.31
2ED020I12-FI	Half-bridge	1200 V	$3.83

disappear (see IKW20N60H3 and IKW25N120H3 in Table II), thereby indicating that the cost saving of symmetrical half-bridge submodules is up to 100% in terms of active switches. In the worst scenario (see IKW50N60T and IKQ50N120CT2), the cost reduction is calculated to be only 8%. However, it is worth noting that active switches are always accompanied by their drivers and peripheral circuits, whose costs must also be counted in.

Table V documents the information of typical IGBT gate drivers from Infineon [31], [32]. Despite price variations, the gate drivers clearly account for an appreciable fraction of semiconductor costs. For example, the 600-V half-bridge driver IR2184S costs $3.32. Taking this into account, one can find that the semiconductor cost reduction of half-bridge submodules is over 17% in the worst-case scenario. In favourable cases, the cost drop approximates 100%. On top of active switches and gate drivers, their peripheral circuits, including heat sinks, driver power supplies, and bootstrap capacitors and diodes, may play an even more important role on converter costs. Arguably, half-bridge submodules eclipse H-bridge submodules with regard to peripheral circuits. From the above analysis, it is safe to conclude that symmetrical half-bridge submodules feature lower semiconductor costs.

It is worthwhile to note that the symmetrical half-bridge submodule involves one more dc capacitor than the H-bridge submodule. For illustration, Fig. 4 presents the cost and energy versus voltage relationships of aluminum electrolytic capacitors from EPCOS(TDK), where capacitance tolerances are within ±20% [33]. In general, the prices of capacitors are in proportion to their stored energies, which are also plotted in Fig. 4 with a factor of 4. Specifically, the prices increase quadratically with voltage ratings and linearly with capacitances. In consequence, dc capacitor costs may outweigh semiconductor costs in high-voltage submodules (e.g., > 400 V in 470 μF cases or > 100 V in 4700 μF cases), thereby making half-bridge-based multilevel converters lose their economic benefits in high-voltage applications. The solution to this challenge will be detailed in Section IV.



(a) 470 μF (b) 4700 μF

Fig. 4. Cost and energy versus voltage relationships of aluminum electrolytic capacitors from EPCOS(TDK) with ±20% capacitance tolerances.

C. Power Loss Analysis

The analysis of power losses is tricky, as it depends on not only power converter topologies and semiconductor switches but also modulation schemes and system operating conditions [34]. To simplify the analysis, we assume that multilevel converters operate with unity power factor and bipolar modulation. In this case, ac voltage and current waveforms are in phase, leading to symmetrical operations with respect to zero-crossing points [35].

Fig. 5 highlights the on-state switches of H-bridge and symmetrical half-bridge submodules in the positive half cycle, where active switches and diodes conduct alternately. Note that the operations of two submodules are very similar. The ac voltage and current without harmonics are expressed as

$$v_{ac}(t)=\sqrt{2}V_{ac}\sin(\omega t),\ i_{ac}(t)=\sqrt{2}I_{ac}\sin(\omega t), \quad (1)$$

where V_{ac} and I_{ac} represent the root-mean-square (rms) values of voltage and current waveforms, respectively.

For H-bridge submodules, the switches T_{H1} and T_{H4} turn on and off simultaneously, and they work alternately with T_{H2} and T_{H3} in a whole cycle. In this way, all the active switches T_{H1}–T_{H4} share the same conduction loss. Their total conduction loss amounts to

$$P_{con\_HT}=\frac{2}{\pi}\int_0^{\pi}\frac{v_{ac}(t)+V_{dc}}{2V_{dc}}i_{ac}(t)v_{T\_on}[i_{ac}(t)]\mathrm{d}(\omega t), \quad (2)$$

where v_{T_on} stands for the on-state voltage drop of T_{H1}–T_{H4}. In (2), the total conduction loss P_{con_HT} is calculated as an aver-

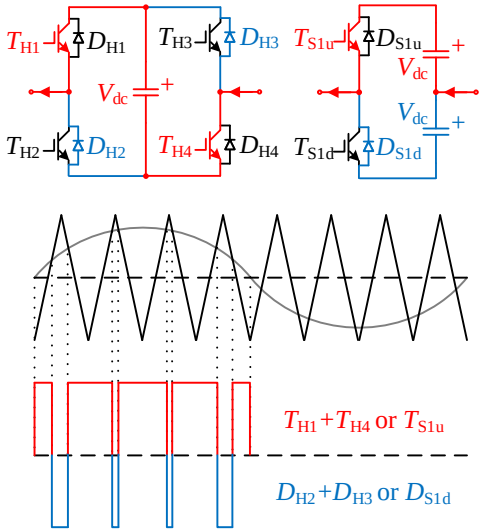


Fig. 5. On-state switches of the H-bridge and symmetrical half-bridge submodules with the unity power factor and bipolar modulation.

age of the voltage drop and current product during on-state periods. Further, v_{T_on} is linearized as

$$v_{T\_on}[i_{ac}(t)] = V_{T0} + R_{T\_on} i_{ac}(t), \quad (3)$$

where V_{T0} and R_{T_on} refer to the zero-current voltage drop and on-state resistor of T_{H1}–T_{H4}, respectively. Note that V_{T0} and R_{T_on} can be obtained from switch datasheets. Similarly, the total conduction loss of diodes D_{H1}–D_{H4} is derived as

$$P_{con\_HD} = \frac{2}{\pi}\int_0^{\pi} \frac{-v_{ac}(t)+V_{dc}}{2V_{dc}} i_{ac}(t) v_{D\_on}[i_{ac}(t)] \mathrm{d}(\omega t), \quad (4)$$

where v_{D_on} designates the diode voltage drop, i.e.,

$$v_{D\_on}[i_{ac}(t)] = V_{D0} + R_{D\_on} i_{ac}(t), \quad (5)$$

where V_{D0} and R_{D_on} denote the zero-current voltage drop and on-state resistor of D_{H1}–D_{H4}, respectively.

The number of on-state switches is halved in half-bridge submodules. To be specific, T_{S1u} or T_{S1d} replaces T_{H1} and T_{H4} or T_{H2} and T_{H3}, respectively. The same holds true for the relevant diodes. Therefore, the conduction losses of half-bridge submodules are expressed as (2) and (4) divided by 2, namely,

$$P_{con\_ST} = \frac{1}{\pi}\int_0^{\pi} \frac{v_{ac}(t)+V_{dc}}{2V_{dc}} i_{ac}(t) v_{T\_on}[i_{ac}(t)] \mathrm{d}(\omega t), \quad (6)$$

$$P_{con\_SD} = \frac{1}{\pi}\int_0^{\pi} \frac{-v_{ac}(t)+V_{dc}}{2V_{dc}} i_{ac}(t) v_{D\_on}[i_{ac}(t)] \mathrm{d}(\omega t), \quad (7)$$

where v_{T_on} and v_{D_on} are given in (3) and (5), respectively. Since v_{ac}, i_{ac}, and V_{dc} are defined by system requirements, the conduction loss mainly differs by the voltage drops v_{T_on} and v_{D_on}, which are partially reflected by $V_{CE(sat)}$ (voltage drops at rated currents) in Table II and $R_{DS(on)}$ (on-state resistances) in Tables III and IV.

Fig. 6 shows the conduction loss ratios of H-bridge submodules to symmetrical half-bridge submodules calculated by (1)–(7), where the datasheets of the switches in Tables II–IV serve as data sources [27–29]. Moreover, the system operating conditions associated with individual switch pairs are designed according to low-voltage switches. Clearly, symmetrical half-bridge submodules reduce conduction losses as compared to H-bridge submodules in all situations. In the worst case (see Si MOS pair 2), symmetrical half-bridge submodules reduce 37% conduction losses. In favorable cases, the saving of conduction losses approximates 100%.

We continue to perform a switching loss comparison. As for H-bridge submodules, the switching loss consists of two parts—the loss of active switches and that related to diodes. All the active switches T_{H1}–T_{H4} share the same switching loss, and their total losses collectively amount to

$$P_{sw\_HT} = \frac{4 f_{sw}}{2} E_{T\_Ts}[i_{ac}(t)], \quad (8)$$

where f_{sw} denotes the switching frequency. E_{T_Ts} comprises the average switching-on and switching-off energies of T_{H1}–T_{H4}. E_{T_Ts} is further calculated as

$$E_{T\_Ts}[i_{ac}(t)] = \frac{1}{\pi}\int_0^{\pi} [E_{T\_Ts0} + A_{T\_Ts} i_{ac}(t)] \mathrm{d}t \text{ or}$$

$$\frac{V_{dc}}{2\pi}\int_0^{\pi} [i_{ac}(t)(T_{MOS\_on} + T_{MOS\_off}) + V_{dc}(C_{MOS\_gd} + C_{MOS\_ds})] \mathrm{d}t \quad (9)$$

for IGBTs and MOSFETs, respectively [20]. In (9), E_{T_Ts0} and A_{T_Ts} are IGBT switching-loss coefficients. T_{MOS_on} and T_{MOS_off} are the switch turn-on and turn-off times of MOSFETs, respectively. C_{MOS_gd} and C_{MOS_ds} are the gate-drain and drain-source capacitances of MOSFETs, respectively. These parameters can be obtained from switch datasheets. In addition, the diode total switching loss is represented as

$$P_{sw\_DT} = \frac{4 f_{sw}}{2} E_{D\_Ts}[i_{ac}(t)], \quad (10)$$

where E_{D_Ts} describes the average switching energy (mainly including the switching-off energy) of each diode, which can be derived as [45]

$$E_{D\_Ts}[i_{ac}(t)] = \frac{V_{dc}}{\pi}\int_0^{\pi} [i_{ac}(t)\frac{I_{D\_rrm}}{\mathrm{d}I_{D\_rr}/\mathrm{d}t} + Q_{D\_rrm}] \mathrm{d}t, \quad (11)$$

where I_{D_rrm}, $\mathrm{d}I_{D\_rr}/\mathrm{d}t$, and Q_{D_rrm} denote the peak reverse recovery current, current recovery rate, and reverse recovery charge, respectively, which can be obtained from datasheets.

In contrast, the number of switches is halved in half-bridge submodules. Correspondingly, the switching loss of active switches and diodes are

$$P_{sw\_ST} = \frac{2 f_{sw}}{2} E_{T\_Ts}[i_{ac}(t)], \quad (12)$$

$$P_{sw\_SD} = \frac{2 f_{sw}}{2} E_{D\_Ts}[i_{ac}(t)], \quad (13)$$

where E_{T_Ts} and E_{D_Ts} are given in (9) and (11) with respective V_{dc} being replaced by $2V_{dc}$ due to increased dc voltage levels.

Fig. 7 demonstrates the switching loss ratios of H-bridge submodules to symmetrical half-bridge submodules, where the datasheets of the switches in Tables II–IV serve as data

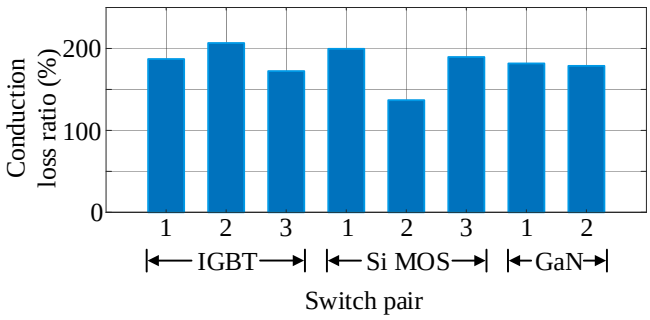


Fig. 6. Conduction loss ratios of H-bridge submodules to symmetrical half-bridge submodules based on the switch pairs in Tables II–IV.

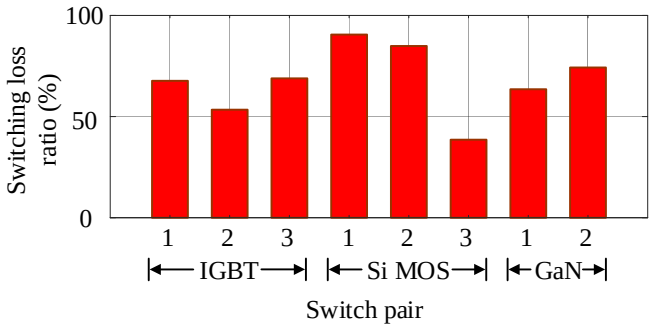


Fig. 7. Switching loss ratios of H-bridge submodules to symmetrical half-bridge submodules based on the switch pairs in Tables II–IV.

sources [27−29]. Generally, symmetrical half-bridge submodules feature higher switching losses as compared to H-bridge submodules. In the worst case, the switching loss of symmetrical half-bridge submodules is 60% higher.

Further, Fig. 8 compares the total power loss ratios of an H-bridge submodule to a symmetrical half-bridge submodule (based on the IGBT switch pair 3) as a function of the switching frequency. In comparison, the symmetrical half-bridge submodule features lower power losses when the switching frequency is relatively low (e.g., < 10 kHz), where the conduction loss dominates.

From the above analyses, it can safely be concluded that the proposed multilevel converters with symmetrical half-bridge submodules feature lower semiconductor costs and conduction losses. By reducing active switch numbers, they exhibit an overwhelming benefit in terms of structure simplicity, which in turn improves system reliability. In particular, the proposed topology is well suited to battery-integrated multilevel converters [20], [36]. It allows control over smaller packs of cells (e.g., balancing of SoC, loss, ageing, power, etc.) with higher-voltage semiconductors instead of tricky low-voltage semiconductors (< 12 V).

IV. Challenges and Solutions of Capacitor Voltage Balance

This section points out the capacitor voltage balance challenge faced by the proposed multilevel converters with symmetrical half-bridge submodules. As a solution, it introduces a novel and effective voltage balance scheme that equalizes capacitor voltages and reduces their ripples.

A. Voltage Balance Challenge

The mismatch between the upper and lower capacitor voltages (see v_{dcxu} and v_{dcxd} in Fig. 3) is an issue peculiar to symmetrical half-bridge submodules and converters. This issue may beget undesirable over-modulation, current distortion, or malfunction of power converters. Capacitance tolerances, dc voltage sensor offsets, and ac current sensor offsets are typical factors causing capacitor voltage imbalances [21].

The injection of a dc component into ac current references is a straightforward solution to the voltage balance issue of half-bridge converters [21], [22], [25]. This solution adds a positive dc component in the output current when the upper capacitor voltage exceeds the lower one. In this way, the discharge and charge times of the upper and lower capacitors increase, respectively, collectively leading to the balance of capacitor voltages.

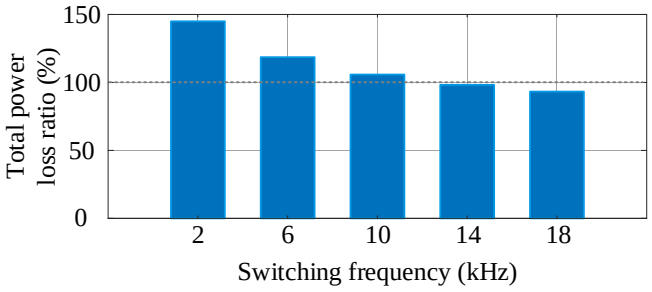


Fig. 8. Total power loss ratios of an H-bridge submodule to a symmetrical half-bridge submodule (based on the IGBT switch pair 3) as a function of the switching frequency.

Unfortunately, the aforesaid solution is not applicable to half-bridge-based multilevel converters. To justify this statement, Fig. 9 displays the control block diagram of grid-tied cascaded-bridge converters with symmetrical half-bridge submodules, where the input signals v_{grid}, v_{dc_ref}, i_{q_ref} represent the grid voltage, capacitor voltage reference, and reactive current reference, respectively. PLL refers to the abbreviation of the phase-locked-loop. $G_{PI}(s)$, $G_{PR}(s)$, $G_{Fil\_1}(s)$, and $G_{Fil\_2}(s)$ stand for the transfer functions of proportional integral (PI) controllers, proportional resonant (PR) controllers, notch filters at the fundamental frequency, and those at the 2nd harmonic, respectively. The output signals d_1, …, d_{n-1}, and d_n, are fed to the pulse width modulators (PWMs) of individual submodules.

As shown in Fig. 9, the overall control block diagram consists of n dc voltage, one current, and one voltage balance control blocks. As the modulation of symmetrical half-bridge and (bipolar modulated) H-bridge submodules are identical, the control block diagram in Fig. 9 largely follows that of single-phase CHB converters except for the voltage balance control [3]. This PWM-based control scheme allows independent dc voltage control. The dc voltage blocks target at the regulation of the capacitor voltage sum in each half-bridge submodule.

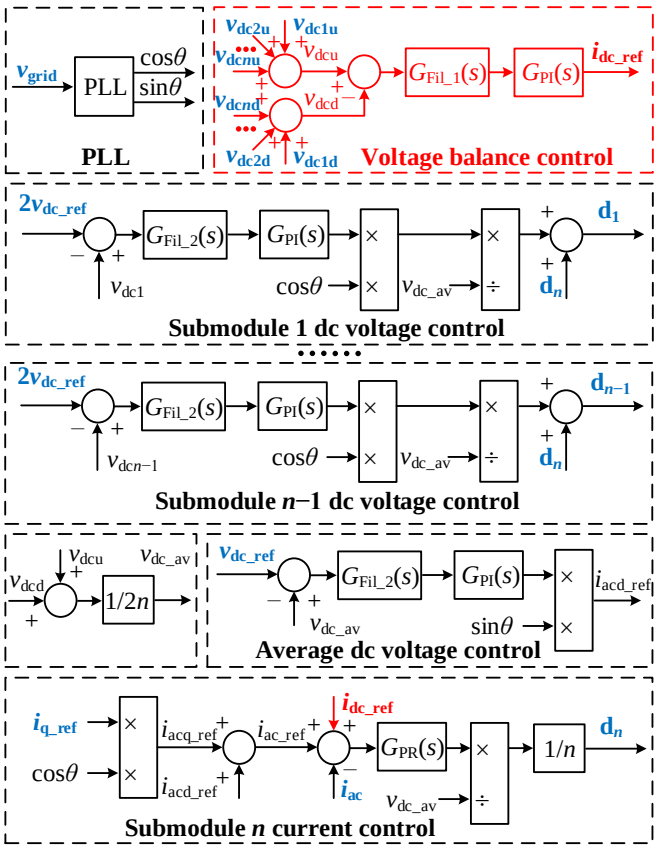


Fig. 9. Control block diagram of grid-tied cascaded-bridge converters with symmetrical half-bridge submodules.

The current block regulates the grid-injected current. Elevated attention should be paid to the voltage balance block, where the error between the upper and lower capacitor voltage sums, i.e., $v_{dcu}-v_{dcd}$, is regulated by a PI controller, whose output i_{dc_ref} subsequently becomes the dc current reference in the current block. This voltage balance control removes voltage imbalances in half-bridge converters [25]. However, it fails to clear the voltage difference in every submodule of multilevel converters, as the current control features only one degree of freedom. Therefore, the voltage balance issue of half-bridge-based multilevel converters remains unsolved.

For validation, Figs. 10 and 11 illustrate Matlab simulation results of voltage balance control in grid-tied half-bridge converters and cascaded-bridge converters, where the system and control parameters are listed in Tables VI and VII, respectively. In Table VII, the control gains of inner-current and outer-voltage loops are tuned following the same design procedure as those of single-phase two-level grid-tied converters and half-bridge converters, as detailed in [22], [37], [38]. Except for the grid voltages (110 Vrms in Fig. 10), the simulation parameters of the two cases are identical. Initially, the upper capacitor voltage in one submodule is intentionally designed to be 50 V greater than the nominal dc voltage 200 V, opposite to the corresponding lower one, while the remaining submodules are with nominal voltages. After the activation of voltage balance control, the half-bridge converter achieves a satisfactory voltage balance. In contrast, the cascaded-bridge converter only equalizes voltage sums, i.e., $v_{dc1u}+v_{dc2u}+v_{dc3u} = v_{dc1d}+v_{dc2d}+v_{dc3d}$, rather than individual voltages.

B. Proposed Voltage Balance Scheme

Fig. 12 presents the proposed voltage balance scheme, where each symmetrical half-bridge submodule employs two additional diodes. Note that the two diodes of the rightmost submodule can be removed for simplicity. These additional diodes D_{S1u}, D_{S1d}, D_{S2u}, and D_{S2d} enable a sensorless balance of all capacitor voltages through submodule parallelization. For instance, the upper capacitor of the second submodule is in parallel with the lower capacitor of the first submodule, when T_{S2u} is turned on, and v_{dc2u} is greater than v_{dc1d}. This parallel connection nulls the difference between v_{dc2u} and v_{dc1d}. Similarly, the voltage mismatch between v_{dc1u} and v_{dc2d} is cleared through D_{S1u} and T_{S2d}. It is worth mentioning that the on-state voltage drops of semiconductors are ignored here. In addition, the idea of voltage balancing via submodule parallelization and its related analysis have been investigated with other MMC topologies [6], [20], [39−41].

As long as the voltage sums of individual submodules are identical, all the capacitor voltages even out. This can be proved with 3 submodules as follows. Under the assumptions that

$$v_{dc1u}+v_{dc1d}=v_{dc2u}+v_{dc2d}=v_{dc3u}+v_{dc3d}=2V_{dc}\,, \tag{14}$$

$$v_{dc1u}+v_{dc2u}+v_{dc3u}=v_{dc1d}+v_{dc2d}+v_{dc3d}\,, \tag{15}$$

Table VI. System parameters of grid-tied cascaded-bridge converters with half-bridge submodules.

Descriptions	Symbols	Values
Fundamental frequency	f_o	50 Hz
Grid voltage (rms)	V_{grid}	220 V
Filter inductance	L_c	10 mH
Nominal dc capacitance	C_{dc}	4700 μF
Nominal dc voltage	V_{dc}	200 V
Submodule number	n	3

Table VII. Control parameters of grid-tied cascaded-bridge converters with half-bridge submodules.

Descriptions	Symbols	Values
Voltage control P gain	K_{vp}	0.5
Voltage control I gain	K_{vi}	5
Current control P gain	K_{cp}	10
Current control R gain	K_{cr}	300
Reactive current reference	I_{q_ref}	30 A
Switching frequency	f_{sw}	10 kHz
Sampling frequency	f_s	10 kHz

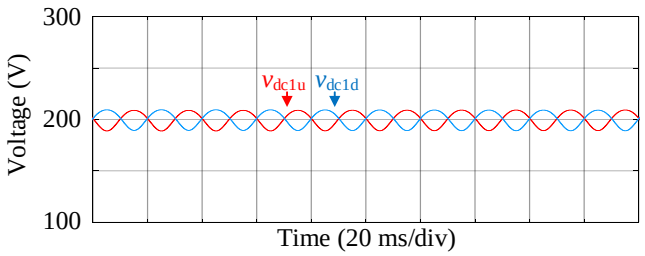


Fig. 10. Simulation results of voltage balance control in the grid-tied half-bridge converter.

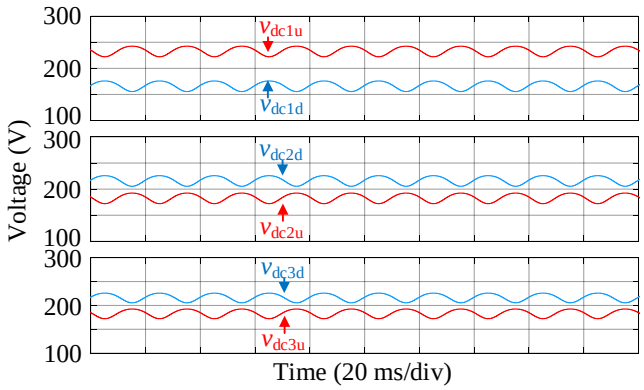


Fig. 11. Simulation results of voltage balance control in the grid-tied cascaded-bridge converter with symmetrical half-bridge submodules.

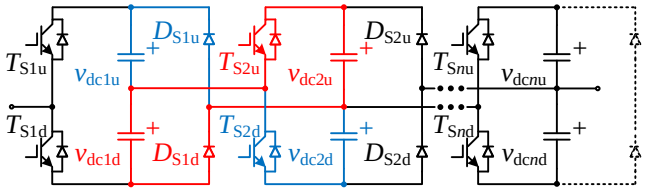


Fig. 12. Schematic of the cascaded bridge converters or MMC arms with symmetrical half-bridge submodules and sensorless voltage balance.

$$v_{dc3d} \geq v_{dc2u} \geq v_{dc1d}\,, \tag{16}$$

$$v_{dc3u} \geq v_{dc2d} \geq v_{dc1u}\,, \tag{17}$$

one can derive

$$v_{dc1u} = v_{dc2d} = v_{dc3u} = v_{dc1d} = v_{dc2u} = v_{dc3d}\,. \tag{18}$$

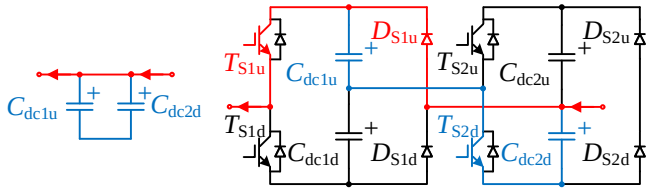
Otherwise, if (18) does not hold valid, the following inequalities will be satisfied by adding (16) and (17),

$$v_{dc3u} + v_{dc3d} > v_{dc2u} + v_{dc2d} \geq v_{dc1u} + v_{dc1d} \quad \text{or} \tag{19}$$

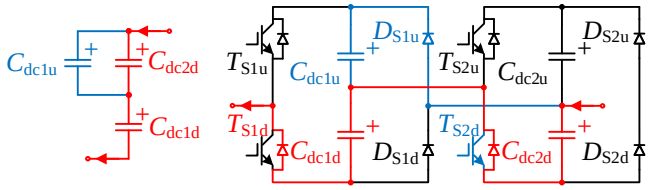
$$v_{dc3u} + v_{dc3d} \geq v_{dc2u} + v_{dc2d} > v_{dc1u} + v_{dc1d}\,, \tag{20}$$

which violate (14). Thus, the proposed scheme achieves the voltage balance goal.

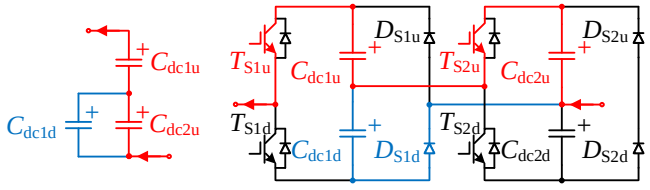
High reliability and sensorless operation are two important benefits of the proposed voltage balance scheme. A further advantage lies in the reduction of voltage ripples. To analyze this, Fig. 13 illustrates the four basic operating modes of the proposed cascaded bridge converters with symmetrical half-bridge submodules and voltage balance scheme. These operating modes are drawn based on several assumptions, including the ignorance of on-state voltage drops, equivalent series resistors, and the conditions where diodes cannot conduct. Let us first focus on the right-hand-side submodule. If its lower switch T_{S2d} turns on [see Fig. 13(a) and (b)], the relevant capacitor C_{dc2d} will be connected in parallel with the upper capacitor C_{dc1u} of the left-hand-side submodule. Furthermore, the two capacitors will continue to parallelize submodules leftwards if T_{s1u} conducts, as shown in Fig. 13(a). Alternatively, Fig. 13(b) indicates that C_{dc2d} and C_{dc1u} will not parallelize leftwards if T_{s1d} conducts. Similarly, Fig. 13(c) and (d) demonstrate the cases where T_{S2u} turns on.



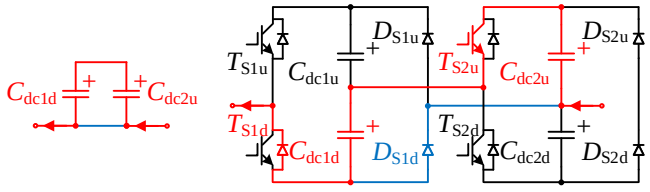
(a) Mode 1



(b) Mode 2



(c) Mode 3



(d) Mode 4

Fig. 13. Operating modes of the cascaded bridge converters or MMC arms with symmetrical half-bridge submodules and sensorless voltage balance.

It can be concluded from the above discussion that the number of paralleled capacitors is influenced by the operating modes of the proposed multilevel converter, which in turn depends on its ac voltage reference. In the most favorable case, all the diagonal capacitors are in parallel, and the resultant current following through each capacitor reduces by a factor of *n*. Correspondingly, the voltage ripple and dc capacitance requirement also decrease by a factor of *n*. The above analysis is well applicable if the ac voltage is relatively low when the ac current reaches its peak, such as in STATCOMs.

According to the circuit theory, the sudden parallelization of two voltage sources (like capacitors) with different voltages is not allowed. However, practical capacitors and switches feature equivalent series resistors (ESRs) and inductors, which attenuate current spikes [6]. Moreover, real switches exhibit forward voltage drops, which are also beneficial for surge current limitations. Detailed analysis of power losses due to parallelization can be found in [6] and [20].

One obvious drawback of the proposed voltage balance scheme refers to the additional cost brought by diodes. Fortunately, diodes are generally much cheaper than the active switches under similar power ratings, as proved by Table VIII [42]. Moreover, diodes operate without drivers or peripheral circuits, and hence save the related costs. More importantly, they deserve the credit for reducing dc voltage ripples and capacitances, and the saving grows as the number of submodules increases. Thus, half-bridge-based multilevel converters can be economically desirable in terms of both passive capacitors and semiconductors.

V. Simulation and Experimental Results

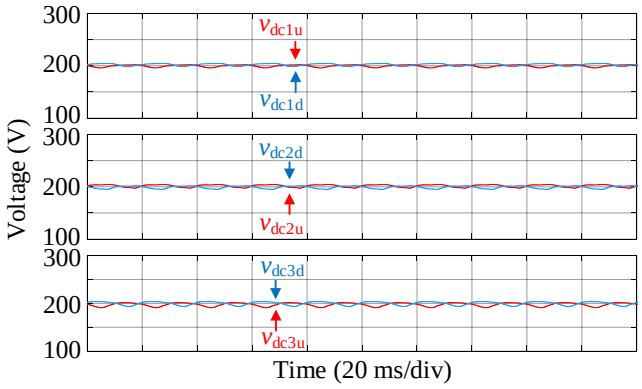
This section provides simulation and experimental results for verification purposes. Simulation results validate the proposed cascaded-bridge converter and voltage balance scheme in both grid-tied static compensator (STATCOM) and islanded battery storage applications, while experimental results focus only on islanded operation.

A. Grid-Tied Operation

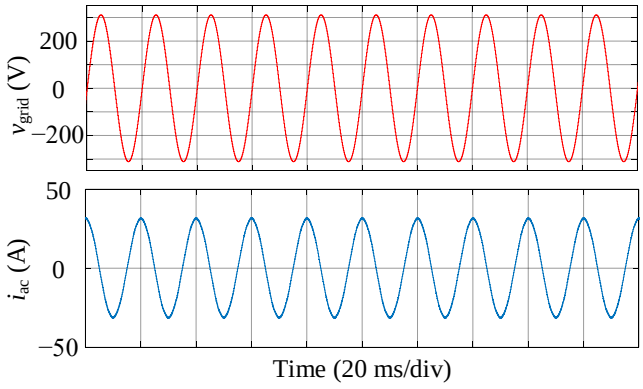
For validation, Fig. 14 shows the steady-state simulation results of the proposed cascaded-bridge converter with symmet-

Table VIII. Infineon silicon power diodes.

Products	Voltage class	V_F	I_F	Prices
IDW50E60	600 V	1.65 V	50 A	$3.34
IDP20E65D2	650 V	1.6 V	20 A	$1.37
IDW40E65D2	650 V	1.6 V	40 A	$3.03
IDB30E120	1200 V	1.65 V	30 A	$2.72

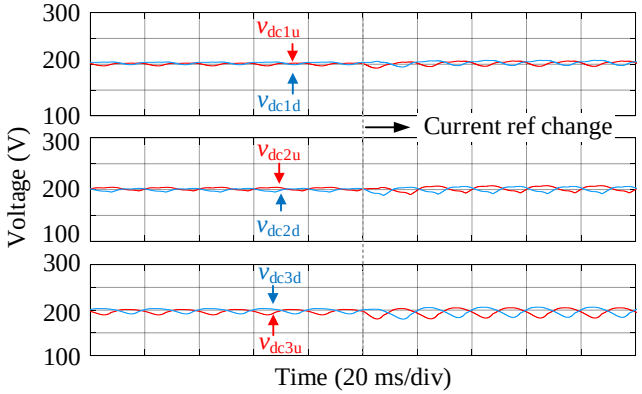


(a) Individual capacitor voltages

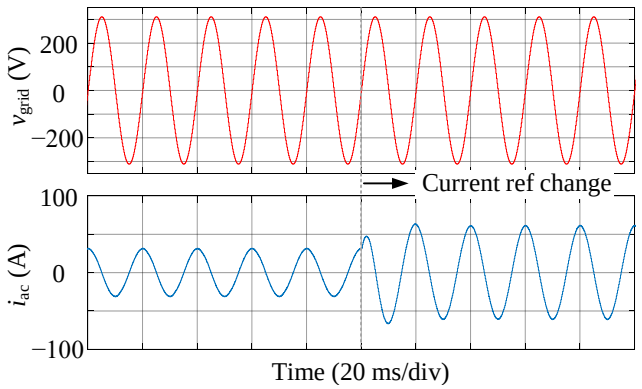


(b) Grid voltage v_{grid} and current i_{ac}

Fig. 14. Steady-state simulation results of the proposed grid-tied cascaded-bridge converter with symmetrical half-bridge submodules.



(a) Individual capacitor voltages



(b) Grid voltage v_{grid} and current i_{ac}

Fig. 15. Transient simulation results of the proposed grid-tied cascaded-bridge converter with symmetrical half-bridge submodules under a step-up current reference change from 30 A to 60 A.

rical half-bridge submodules in grid-tied applications, where the system and control parameters are listed in Tables IV and V, respectively. Fig. 14(a) reveals that the target of voltage balance is achieved even with different initial capacitor voltages. As compared to Fig. 11, a great reduction of voltage ripples (peak to peak) from 20 V to less than 10 V is expected, thereby demonstrating the saving of more than 50% capacitances under the same ripple condition. Fig. 14(b) demonstrates the waveforms of the grid voltage v_{grid} and current i_{ac}, where i_{ac} leads v_{grid} by 90 degrees for reactive power compensation. Clearly, the proposed multilevel converter operates well as a STATCOM.

Fig. 15 shows the transient simulation results of the proposed cascaded-bridge converter with symmetrical half-bridge submodules under a step current reference change from 30 A to 60 A. As shown in Fig. 15(a), individual capacitor voltages are balanced and well regulated. Moreover, it is clear from Fig. 15(b) that the grid current i_{ac} accurately tracks its reference within one line cycle, thereby demonstrating the satisfactory dynamics of the proposed converter.

B. Islanded Operation

In this subsection, the proposed cascaded-bridge converter serves to integrate battery storage and supply a resistive load. As such, all submodules are designed with low-voltage ratings for dynamically reconfigurable battery circuits. The corresponding system parameters are given in Table IX.

Fig. 16 visualizes the experimental prototype. The major experimental devices include an oscilloscope (MDO3054: 500 MHz, 2.5 GS/s), three submodules with MOSFETs (IPT015N10N5: 100 V, 300 A) and their drivers (Si8233: 4.0 A), batteries (AJC D1.3S: 12V, 1.3Ah), aluminum electrolytic capacitors (ESK108M063AM7AA: 100 V, 1000 μF), and a development board (TI TMS03XF3F04jD) of digital signal processors (DSP TMS320F28379D: 200 MHz) [43], [44].

Figs. 17 and 18 illustrate the simulation and experimental results of the cascaded-bridge converter with symmetrical half-bridge submodules, respectively, but without the pro-

Table IX. System parameters of islanded cascaded-bridge converters with half-bridge submodules.

Descriptions	Symbols	Values
Fundamental frequency	f_o	50 Hz
Switching frequency	f_{sw}	10 kHz
Load resistance	R_l	10 Ω
Filter inductance	L_c	10 mH
Nominal dc capacitance	C_{dc}	1000 μF
Battery voltage	$2V_{dc}$	12.5 V
Submodule number	n	3

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2020.3000469, IEEE Transactions on Power Electronics

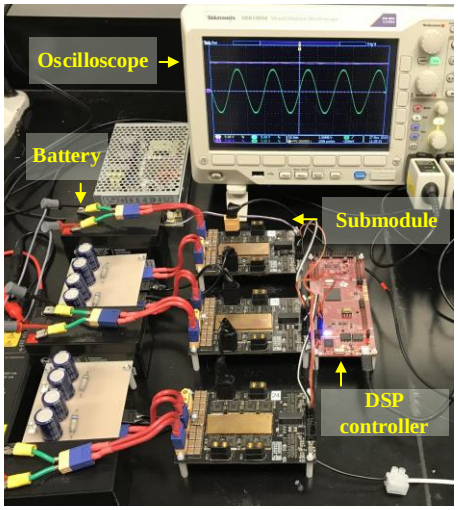


Fig. 16. Photo of the experimental prototype.

posed voltage balance scheme. In this case, the lower capacitor of the third submodule is intentionally designed with its capacitance doubled, i.e., 2000 μF, to yield an imbalance condition. As anticipated, the individual capacitor voltages differ from each other (see v_{dc3u} and v_{dc3d}). Another observation is that the maximum voltage ripple (peak to peak) reaches 1.6 V. Additionally, it should be commented that we remove the switching ripples in the oscilloscope to give clear waveforms.

Figs. 19 and 20 present the simulation and experimental results of the cascaded-bridge converter with symmetrical half-bridge submodules and voltage balance diodes, where $v_{dcx\_sum} = v_{dcxu} + v_{dcxd}$ (x = 1, 2, or 3) stands for the voltage sum in each submodule. Obviously, the balance of all capacitor voltages is perfectly achieved with an efficiency of 98.1%. Moreover, the maximum voltage ripple is limited to be around 0.6 V. Notably, the load voltage v_{load} exhibits a clean sinusoidal waveform with a low total harmonic distortion (THD) < 1% due to the shifted phases of modulation signals. The above simulation and experimental results agree well with the theoretical analysis.

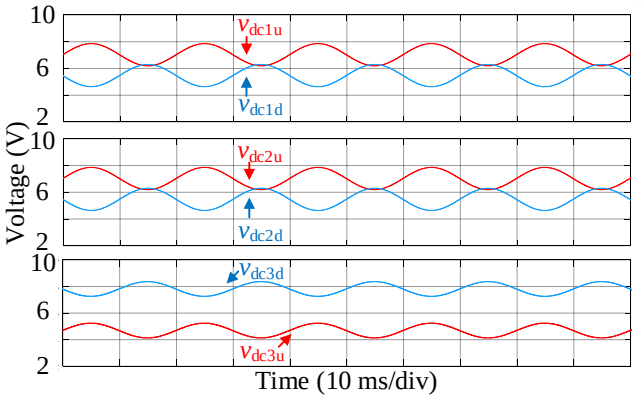


Fig. 17. Simulation results of the islanded cascaded-bridge converter with symmetrical half-bridge submodules and without voltage balance.

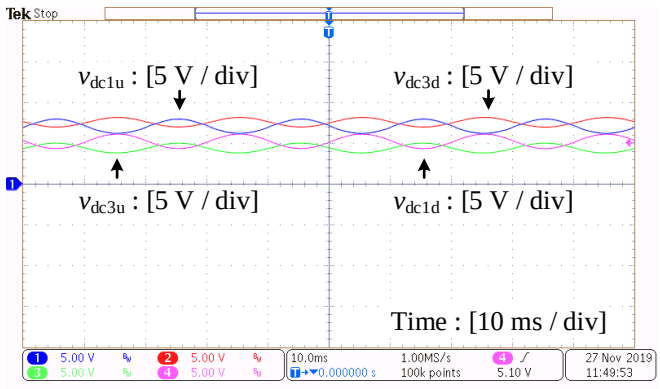
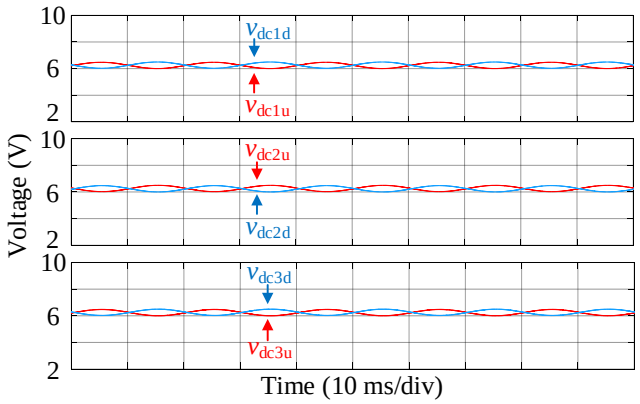


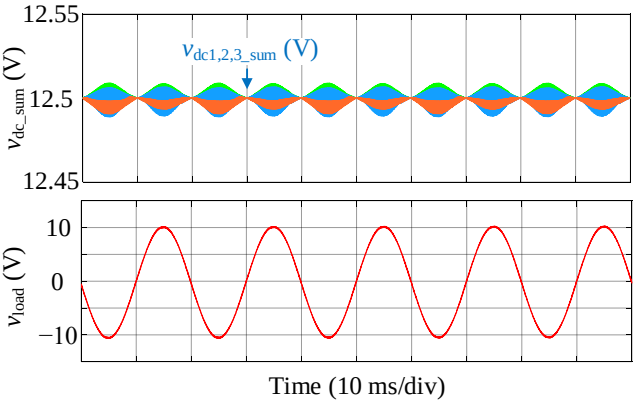
Fig. 18. Experimental results of the islanded cascaded-bridge converter with symmetrical half-bridge submodules and without voltage balance.

VI. Conclusions

This paper has proposed novel multilevel converter family with symmetrical half-bridge submodules. This family offers low costs and conduction losses as well as great simplicity and reliability. Through the addition of diodes, the proposed voltage balance scheme provides added incentives, as it translates into the removal of voltage sensors and saving of dc capacitances. The proposed voltage balance scheme is particularly of interest in the applications where a huge number of submodules in multilevel converters is expected. Finally, the simula-

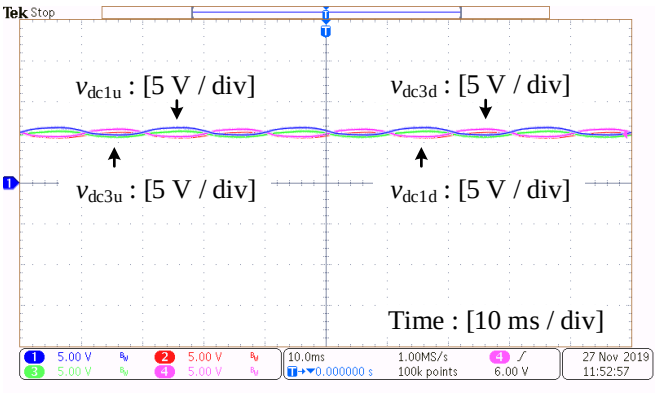


(a) Individual capacitor voltages

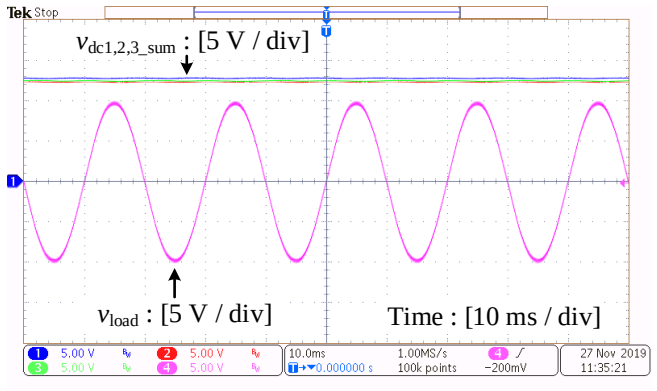


(b) Capacitor voltage sums v_{dcx_sum} (x = 1, 2, or 3) and load voltage v_{load}

Fig. 19. Simulation results of the islanded cascaded-bridge converter with symmetrical half-bridge submodules and voltage balance.



(a) Individual capacitor voltages



(b) Capacitor voltage sums v_{dcx_sum} (x = 1, 2, or 3) and load voltage v_{load}

Fig. 20. Experimental results of the islanded cascaded-bridge converter with symmetrical half-bridge submodules and voltage balance.

tion and experimental testing of the proposed multilevel converters and voltage balance scheme is performed, which shows a good agreement with the theoretical analysis.

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